REMARKS

By this amendment claim 5 has been amended. Claims 1-11 remain pending. Reconsideration of the application as amended is respectfully requested.

Rejections under 35 USC §102(b)

Claims 1-3, 5, 7 have been rejected under 35 USC §102(b) as being unpatentable over Miyakawa (US 6,235,619). Miyakawa describes the formation of a MOSFET device comprising several columns of transistors, with transistors of five different columns being depicted at FIG. 9. The transfer gates of two of these columns are depicted in FIG. 13, and are numbered "104" in FIGS. 7 and 13, but are not individually numbered in FIG. 9. As is known in the art, structures 104 of FIG. 13, which are referred to as "transfer gates" by Miyakawa (column 5 line 37), each have a plurality of individual transistors therealong using a configuration of field oxide and active area doping regions.

FIG. 8 depicts an opening 113 which exposes a doped region within the wafer 101. The exposed doped region forms a shared active region for the adjacent transistors depicted in FIG. 9. A conductive layer 114 (FIG. 9) is provided within the opening.

It appears that the conductive layer 114, depending on where it is formed, is used as an electrode to connect a bottom storage plate to the substrate (column 7 lines 1-5) and as a bit line contact (column 7 lines 58-60). FIG. 13 appears to depict two plugs, with the plug at d3 providing a connection for the storage capacitor bottom plate to the wafer, and the plug at d1 providing a digit (bit) line contact to the wafer. The light grey region which is unnumbered but extends generally horizontally appears to be the active area.

As described above, a plurality of transistors are located between each transfer gate 104 of FIG. 13, with only one active area being shown in FIG. 13 (in light grey). As can be determined from FIG. 13, each plugs 113 is connected to only one doped wafer region (one active area). FIG. 13 does not depict the plug 113 extending to other source regions between the two transfer gates 104 depicted.

The Examiner states that Miyakawa teaches that each "said conductive line electrically couples each said source region of each transistor in each of two columns of transistors" and refers to FIGS. 6-12 and col. 6-line 17 to col. 9-line 7. However, the text and FIGS. only depict each plug contacting one source/drain region. Layer 113 does not extend to multiple sources, at least because layer 113 is used as either an electrode to connect a bottom storage plate to the substrate (column 7 lines 1-5) or as a bit line contact (column 7 lines 58-60). Thus it is not possible for layer 113 to "electrically couple[s] each said source region of each said transistor in each of said two columns of transistors" as recited in claim 1, at least because it would produce a nonfunctional device having all storage capacitor bottom electrodes along two adjacent transfer gates shorted together, or having the digit lines shorted to the source region. Further, Miyakawa does not appear to recite "at least two columns of transistors *within a single sector*" of a memory device, as Miyakawa does not appear to discuss sectors at all (which are an element of flash memory devices). Thus claim 1 and rejected claims 2 and 3 which depend therefrom are allowable over Miyakawa.

Rejected claims 5 and 7 also comprise novel and nonobvious difference over Miyakawa. The Examiner uses layer 105 to teach the "blanket etch-resistant layer" of present claim 5 and the dielectric layer 110 to teach the dielectric layer. While many of the elements of the present rejected claims may be depicted in Miyakawa, they are not depicted at the same time, are mutually exclusive, and thus do not fulfill the requirements necessary for proper rejection under 35 USC §102(b).

Claim 5 recites "a gate oxide layer extending from under said control gate of said first transistor control gate, to under said second transistor control gate; a first spacer contacting said first transistor control gate and a second spacer contacting said second transistor control gate; a blanket etch-resistant layer which contacts said gate oxide layer...and said first and second spacers...; a dielectric layer which contacts said blanket etch-resistant layer at said location between said first and second transistors, said dielectric layer comprising: a first upper surface which is at a level below said horizontally-oriented surface of said capping layer; a second upper surface which is at a level above said horizontally-oriented upper surface of said capping layer; a first vertically-oriented sidewall which overlies said first transistor control gate; and a second vertically-oriented sidewall which overlies said second transistor control gate, wherein a portion of said etch-resistant layer is not covered by said dielectric layer."

It can be determined that there is no instant in time when this claimed structure is present in Miyakawa. For example, dielectric layer 110 contacts etch-resistant layer 105 between the first and second transistor, but only prior to its etching to form the FIG. 7 structure; after etching to form the FIG. 7 structure, it does not contact layer 105 between the two transistors. However, prior to etching layer 110, there is no first sidewall which overlies the first transistor nor a second sidewall which overlies the second transistor. After forming the sidewalls, the dielectric layer 110 does not contact layer 105 between the transistors. Once layer 105 is etched, it is no longer a blanket layer as presently claimed. During the etch of layer 110 to form the structure of FIG. 7 a portion of layer 110 may remain between the two transistors, but FIG. 7 does not have a first spacer which contacts the first transistor control gate or a second spacer which contacts the second transistor control gate, with the etch-resistant layer contacting the first and second spacers.

Claim 7 is further allowable over Miyakawa under 35 USC §102(b). Claim 7 recites "a first spacer which contacts said first vertically-oriented sidewall of said dielectric layer; and a second spacer which contacts said second vertically-oriented sidewall of said dielectric layer, wherein said first upper surface of said dielectric layer is exposed." After forming spacers 112 of FIG. 8, layer 105 is not a blanket layer as presently claimed, but has been etched. Thus claims 5 and 7 which have been rejected under 35 USC §102(b) are allowable over Miyakawa.

Rejections under 35 USC §103(a)

Claim 4 has been rejected over Miyakawa and official notice in combination. As discussed relative to the rejections under 35 USC §102(b), the recitations of claim 1 from which claim 4 depends are not taught by Miyakawa, for example a conductive line which "electrically couples each said source region of each transistor in each of two columns of transistors." Thus all of the limitations of claim 1 from which claim 4 depends are not taught as required (MPEP §706.02j), and claim 4 is allowable under 35 USC §103(a) for at least this reason.

Claims 8-11 have been rejected under 35 USC §103(a) over Miyakawa and Lee (US 5,270,240) in combination. Miyakawa describes a semiconductor device having first and second transfer gates 104, a diffusion region (not individually numbered, within 101 at FIG. 8), a gate oxide layer, first and second spacers (not numbered, at FIG. 8, neither of which contact the transfer gate 104), an etch resistant layer 105 which contacts unnumbered spacers at FIG. 8. Lee at FIG. 14 depicts first and second word lines 10, a source diffusion region 16, a gate oxide layer 92, first and second spacers 130 which contact the word lines 10, an etch resistant layer 140, and an etch mask having an opening therein.

The rejected claims comprise novel and nonobvious differences over the invention of Miyakawa and Lee in combination. While many of the elements of the present rejected claims may be depicted in Miyakawa and Lee, they are not depicted at the same time, are mutually exclusive, and thus do not fulfill the requirements necessary for proper rejection under 35 USC §103(a). For example, claim 8 recites "a first spacer which contacts said first word line and a second spacer which contacts said second word line; an etch-resistant layer which contacts said first spacer, said second spacer, and said gate oxide layer and which defines a recess over said source diffusion region; a dielectric layer formed within said recess over said source diffusion region; and an etch mask having an opening therein which exposes said dielectric layer.

With Miyakawa, layer 105 contacts the transfer gates 104, and thus must be used as the first and second spacers. However, after etching layer 105 to provide spacers, gate oxide layer does not appear to extend "from under said first word line, across said source diffusion region, to under said second word line." If the gate oxide extended across the plug 113 would not make electrical contact with the doped region in wafer 101. It also appears that with Lee, after etching spacer layer 120 to form spacers 130, the gate oxide 92 does not extend continuously from under one gate to the other gate. Further, with Miyakawa, the only dielectric layer formed after etching layer 105 to form the spacers appears to be the layer which forms spacers 112. However, there is no simultaneous existence of an "etch-resistant layer which contacts said first spacer, said second spacer, and said gate oxide layer and which defines a recess over said source diffusion region" and "a dielectric layer formed within said recess over said source diffusion region." Immediately after forming layer 112 which defines a recess, it is etched, thus no dielectric layer is formed simultaneous with its defining of a recess. Lee at FIG. 14 depicts an etch stop layer 140, but does not have a dielectric layer formed therein along with an etch mask having an opening therein which exposes said dielectric layer. Lee depicts only spacers 130 contacting word line 10, an etch stop layer 140, and etch mask 142.

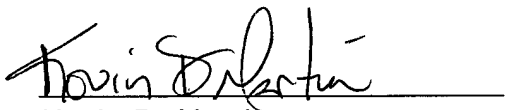
Additionally, the Examiner uses layer 140 to teach an "unetched spacer layer," however layer 140 is never etched to form a spacer, functions as an etch stop layer, and thus would be more accurately described as an etch stop layer than a spacer layer.

Finally, the combination of references to result in the present invention as claimed is not possible. Lee describes the formation of a digit line (180) and of a source line (160), while Miyakawa describes the formation of a storage capacitor contact (113 at d3) and a digit line contact (113 at d1). Thus there is no motivation to combine the references. The flash device of Lee does not need a storage capacitor contact, as it uses a floating gate structure, and it already has a digit line contact. It is not evident that the formation of the digit line contact of Miyakawa would improve the process of Lee. Thus the combining of references to result in the present invention as claimed is respectfully traversed. Claims 8-11 are therefore allowable under 35 USC §103(a)over Miyakawa and Lee in combination.

Conclusion

If there are matters which may be clarified or resolved through a telephone call, the Examiner is cordially invited to contact the undersigned. This is believed to be a complete and proper response to the Examiner's office action.

Respectfully submitted,



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